

J007 Rec'd PCT/PTO 27 MAR 2001

ATTORNEY'S DOCKET NO: 010288

U.S. DEPARTMENT OF COMMERCE, PATENT AND TRADEMARK OFFICE		DATE: March 27, 2001
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLN. NO. (if known): 09/806054
INTERNATIONAL APPLICATION NO.: PCT/JP00/05629	INTERNATIONAL FILING DATE: AUGUST 23, 2000	PRIORITY DATE CLAIMED: SEPTEMBER 21, 2000
TITLE OF INVENTION: PLL CIRCUIT		
APPLICANT(S) FOR DO/EO/US: Takushi KIMURA and Masamichi NAKAJIMA		
Applicant hereby submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:		
<p>1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.</p> <p>2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.</p> <p>3. <input checked="" type="checkbox"/> This express request to begin national examination procedures (35 USC 371(f)) at any time rather than delay examination until the expiration of the time limit set in 35 USC 371(b) and PCT Articles 22 and 39(1).</p> <p>4. <input type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.</p> <p>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2)):</p> <p style="margin-left: 20px;">a. <input checked="" type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau).</p> <p style="margin-left: 20px;">b. <input type="checkbox"/> has been transmitted by the International Bureau.</p> <p style="margin-left: 20px;">c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US)</p> <p>6. <input checked="" type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)).</p> <p>7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))</p> <p style="margin-left: 20px;">a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau).</p> <p style="margin-left: 20px;">b. <input type="checkbox"/> have been transmitted by the International Bureau.</p> <p style="margin-left: 20px;">c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</p> <p style="margin-left: 20px;">d. <input checked="" type="checkbox"/> have not been made and will not be made.</p> <p>8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</p> <p>9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</p> <p>10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).</p> <p>ITEMS 11. TO 16. BELOW CONCERN OTHER DOCUMENT(S) OR INFORMATION INCLUDED:</p> <p>11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98 together with the international search report and 2 references..</p> <p>12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. ASSIGNEE NAME AND ADDRESS: FUJITSU GENERAL LTD, Kawasaki, Japan</p> <p>13. <input type="checkbox"/> A FIRST preliminary amendment. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment</p> <p>14. <input type="checkbox"/> A substitute specification.</p> <p>15. <input type="checkbox"/> A change of power of attorney and/or address letter.</p> <p>16. <input checked="" type="checkbox"/> Other items or information: 4 sheets of drawings.</p>		

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U.S. APPLICATION NO. (if known) 09/806054		INTERNATIONAL APPLICATION NO. PCT/JP00/05629		DATE: March 27, 2001	
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<p>17. <input checked="" type="checkbox"/> The following fees are submitted:</p> <p>Basic National Fee (37 CFR 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO: \$860.00</p> <p>International preliminary examination fee paid to USPTO (37 CFR 1.482) \$690.00</p> <p>No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) \$710.00</p> <p>Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$1000.00</p> <p>International preliminary examination fee (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) \$100.00</p> <p style="text-align: right;">ENTER APPROPRIATE BASIC FEE AMOUNT = \$ 860.00</p>	<p><u>CALCULATIONS</u></p>	<p><u>PTO USE ONLY</u></p>
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Surcharge of \$130.00 for furnishing the oath or declaration later than <u>x</u> 20 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	\$ 130.00	
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CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
TOTAL	12 - 20 =		X \$ 18.00		
INDEPENDENT	1 - 3 =		X \$ 80.00		
Multiple dependent claims(s) (if applicable)			+ \$270.00	\$ 270.00	
TOTAL OF ABOVE CALCULATIONS =				\$ 1,260.00	
Reduction by 1/2 for filing by small entity, if applicable. (Note 37 CFR 1.9, 1.27, 1.28).					
SUBTOTAL =				\$12,60.00	
Processing fee of \$130.00 for furnishing the English translation later than <u> </u> 20 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				+	
TOTAL NATIONAL FEE =				\$1,260.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +					
TOTAL FEES ENCLOSED =				\$ 1,260.00	
				Amount to be:	
				refunded	\$
				charged	\$

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a. XX A check in the amount of \$ **1,260.00** to cover the above fees is enclosed. (\$860.00 for filing fee; \$270.00 for multiple dependent claims and \$130.00 for late filing of the declaration). (This paper is filed in triplicate)

b. Please charge my Deposit Account No. 01-2340 in the amount of \$ to cover the above fees. (A duplicate copy of this sheet is enclosed.)

c. X The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2340.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed to request that the application be restored to pending status.

Send All Correspondence To:


23850
 PATENT TRADEMARK OFFICE

William L. Brooks

 SIGNATURE

William L. Brooks

 NAME

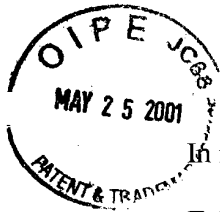
34,129

 REGISTRATION NUMBER

WLB/yap

ARMSTRONG, WESTERMAN, HATTORI,
 McLELAND & NAUGHTON, LLP
 Suite 1000, 1725 K Street, N W
 Washington, D C 20006
 Tel: (202) 659-2930
 Fax: (202) 887-0357

JG17 Rec'd PCT/PTO 25 MAY 2001



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

[Handwritten signature]

In re the Application of:

Takushi KIMURA et al.

Serial Number: 09/806,054

Group Art Unit: Unassigned

Filed: March 27, 2001

Examiner: Unassigned

For: PLL CIRCUIT

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

May 25, 2001

Sir:

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Amend the specification as follows:

Please replace the paragraph beginning at page 11, line 24 with the following rewritten paragraph:

Further, in the above description, the operation stoppage state of the PLL circuit is judged by the presence/absence of an output signal of the frequency divider 4. However, the operation stoppage state of the PLL circuit may be judged by detecting whether or not the oscillation frequency fck of the voltage control oscillator 3 is a frequency of a predetermined value or more. In [the later]

U.S. Patent Application Serial No. 09/806,054

this case, the signal of the frequency fck may be converted into a voltage signal by a frequency/voltage converter, and this voltage signal compared with a predetermined value by a voltage comparator.

IN THE CLAIMS:

Cancel claim 3.

Amend claim 1 as follows:

1. (Amended) A PLL circuit in which a phase comparator, a loop filter, a voltage control oscillator and a frequency divider are successively loop-connected, said PLL circuit comprising:

operation stoppage detecting means for detecting that PLL operation has stopped, said detection being effected on the basis of an output signal from said voltage control oscillator or said frequency divider; and

control means for, when said operation stoppage detecting means detects stoppage of operation, controlling the voltage control oscillator such that an oscillation frequency of the voltage control oscillator is low.

U.S. Patent Application Serial No. 09/806,054

REMARKS

Claims 1-2 and 4-6 are pending in this application, of which claim 1 has been amended.
Claim 3 has been canceled. No new claims have been added.

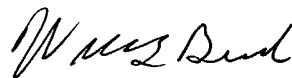
The claims are now in condition for examination.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON, LLP



William L. Brooks
Attorney for Applicants
Reg. No. 34,129

Atty. Docket No. 010288
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 659-2930
WLB:mlg
Enclosures: Version With Markings To Show Changes Made

U.S. Patent Application Serial No. 09/806,054

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The specification has been amended as follows:

Paragraph beginning at line 24 of page 11 has been amended as follows:

Further, in the above description, the operation stoppage state of the PLL circuit is judged by the presence/absence of an output signal of the frequency divider 4. However, the operation stoppage state of the PLL circuit may be judged by detecting [by a separately provided voltage comparator whether or not the control voltage V_a of the voltage control oscillator 3 is less than or equal to a predetermined level, or by detecting] whether or not the oscillation frequency f_{ck} of the voltage control oscillator 3 is a frequency of a predetermined value or more. In [the later] this case, the signal of the frequency f_{ck} may be converted into a voltage signal by a frequency/voltage converter, and this voltage signal compared with a predetermined value by a voltage comparator.

In the Claims:

Claim 3 has been canceled.

Claim 1 has been amended as follows:

4/PRTS

09/806054

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SPECIFICATION

PLL CIRCUIT

Technical Field

The present invention relates to a PLL circuit which generates and outputs a frequency signal which has a predetermined relationship with a reference frequency signal, and in particular, to a PLL circuit which enacts countermeasures in cases in which PLL operation stops.

Background Technology

As illustrated in Fig. 7, in a PLL circuit, phases of a reference signal f_r and a comparison signal f_c are compared at a phase comparator 101 which is formed by an exclusive OR circuit or the like. The signal of the results of comparison is smoothed at a loop filter 102 to become a control voltage V_c . The frequency oscillated by a voltage control oscillator (VCO) 103 is controlled by this control voltage V_c , and the frequency signal f_{ck} obtained thereat is the output frequency signal. This output frequency signal f_{ck} is inputted to a frequency divider 104, and there, the frequency is made to be $1/N$ and the resulting signal is inputted as the comparison signal f_c to the phase comparator 101.

At the PLL circuit, the entire circuit is operated such that, given that the frequency of the reference signal f_r is f_r , the frequency of the comparison signal f_c is f_c , and the frequency of the oscillation frequency signal f_{ck} is f_{ck} , in a

synchronized state, the relational formulas

$$f_r \cong f_c, f_c = f_{ck}/N$$

are satisfied, such that the comparison signal f_c always follows the reference signal f_r .

When an analog image signal is digitally processed, a PLL circuit such as that described above is used in order to generate a sampling clock. The frequency of the sampling clock extends over a wide range of from 10MHz to 100MHz or more depending on the type of image signal.

Therefore, there are cases in which it is demanded of the voltage control oscillator 103 that the maximum/minimum frequency ratio of the oscillation frequency thereof is two times or more, and that the oscillation frequency is greater than or equal to 200MHz. A voltage control oscillator of a wide frequency range that can cover such cases is used.

However, in a PLL circuit having a voltage control oscillator of such a wide frequency range, when the oscillation frequency is higher than needed, the circuit of a portion which forms the PLL circuit may not be able to follow, and PLL operation may stop. Such a situation occurs, for example, when the reference signal f_r changes suddenly (the input signal becomes on/off, or the like) and the oscillation frequency varies greatly until a synchronized stable state is reached, or when the frequency of the reference signal f_r is increased greatly and the oscillation frequency is increased, and the like.

In such cases, the frequency dividing operation of the frequency dividing circuit 104 is not able to follow, and the

output signal, i.e., the comparison signal f_c , disappears. Thus, the phase comparator 101 judges that the oscillation frequency of the voltage control oscillator 103 has fallen, operates such that the oscillation frequency is increased, and boosts the control voltage V_c to the maximum oscillation frequency. When such a state arises, even if this state is temporary, it is impossible for operation to return to normal by itself.

Therefore, conventionally, in order to have the oscillation frequency f_{ck} of the voltage control oscillator 103 not exceed the operating limit frequencies of the other circuits forming the PLL circuit, a voltage limiting circuit 105 such as that illustrated in Fig. 8 was inserted between the voltage control oscillator 103 and the loop filter 102, so as to provide an upper limit for the control voltage V_c .

In the voltage limiting circuit 105 of Fig. 8, the maximum value of the control voltage V_c is limited by a voltage-regulator diode ZD , and, as illustrated in Fig. 9, the oscillation frequency of the voltage control oscillator 103 is limited to f_d which is sufficiently lower than the maximum value f_{max} . As a result, the frequency f_{ck} , which oscillates at the voltage control oscillator 103, is in the range from the minimum frequency f_{min} to the upper limit frequency f_d , and the above-described problem can be avoided.

However, in a method in which the control voltage V_c inputted to the voltage control oscillator 103 is directly limited by the voltage limiting circuit 105 in this way, there were the problems that the dispersion in the characteristics

of the voltage-regulator diode ZD which is the limiting element of the voltage limiting circuit 105, and the dispersion in the oscillation frequency f_{ck} at the voltage control oscillator 103 with respect to the control voltage V_c , had to be newly corrected, and further, that the oscillation frequency of the PLL circuit had to be limited with sufficient margin from the operation frequency (target frequency) of the PLL circuit.

Therefore, an object of the present invention is to provide a PLL circuit which can easily return to normal, even if the voltage control oscillator oscillates abnormally and PLL operation stops.

DISCLOSURE OF THE INVENTION

In the present invention, a PLL circuit in which a phase comparator, a loop filter, a voltage control oscillator and a frequency divider are successively loop-connected, comprises: operation stoppage detecting means for detecting that PLL operation has stopped; and control means for, when said operation stoppage detecting means detects stoppage of operation, controlling the voltage control oscillator such that an oscillation frequency of the voltage control oscillator is low. In this way, when the oscillation frequency of the voltage control oscillator exceeds a predetermined value and the PLL circuit stops operating, operation can quickly be returned to normal by a simple structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a PLL circuit of a first embodiment of the present invention.

Fig. 2 is a block diagram of a comparison signal presence/absence detector.

Fig. 3 is a timing chart of operation of the comparison signal presence/absence detector.

Fig. 4 is a block diagram of a phase comparator.

Fig. 5 is an operation characteristic diagram of forced return of a voltage control oscillator at the time of abnormal oscillation.

Fig. 6 is a block diagram of a PLL circuit of a second embodiment of the present invention.

Fig. 7 is a block diagram of a conventional, general PLL circuit.

Fig. 8 is a circuit diagram of a voltage limiting circuit.

Fig. 9 is a characteristic diagram of oscillation frequency with respect to control voltage of the voltage control oscillator.

PREFERRED EMBODIMENT FOR IMPLEMENTING THE INVENTION

Fig. 1 is a block diagram of a PLL circuit of an embodiment of the present invention. 1 is a phase comparator which compares phases of a reference signal f_r and a comparison signal f_c and outputs a signal which corresponds to the results of the comparison, 2 is a loop filter which smoothes the comparison signal, 3 is a voltage control oscillator which oscillates a signal f_{ck} of a frequency which is proportional to an inputted

control voltage V_c , 4 is a frequency divider which frequency-divides the frequency of an inputted signal into $1/N$, and 5 is a comparison signal presence/absence detector (operation stoppage detecting means) which detects the presence/absence of the comparison signal f_c .

In this way, in the present embodiment, the comparison signal presence/absence detector 5 is connected to the output side of the frequency divider 4. When it is detected there that there is no comparison signal f_c , the signal outputted from the phase comparator 1 is a signal which controls the oscillation frequency f_{ck} of the voltage control oscillator 3 to a low frequency.

Fig. 2 is a block diagram which illustrates the internal structure of the comparison signal presence/absence detector 5. 51, 52 are DFF circuits, and 53, 54 are inverters. Here, a high level signal is inputted to the D terminal of the DFF circuit 51, and a test signal f_t generated independently (and having a frequency less than or equal to $1/2$ of the comparison signal f_c and a duty ratio of 50%) is inputted to the CK terminal of the DFF circuit 51. The comparison signal f_c is inputted to the R (reset) terminal of the DFF circuit 51 via the inverter 54. Further, in the DFF circuit 52, a signal from the Q1 terminal of the DFF circuit 51 is inputted to the D terminal of the DFF circuit 52, and the test signal f_t is inverted at the inverter 53 and inputted to the CK terminal of the DFF circuit 52.

Fig. 3 is a timing chart of operation of the comparison signal presence/absence detector 5. Each time the test signal

ft rises, the Q1 terminal of the DFF circuit 51 senses a high level of the D terminal and becomes a high level. When the comparison signal fc rises, the Q1 terminal of the DFF circuit 51 is reset and becomes a low level. The DFF circuit 52 outputs, to the Q2 terminal, data of the D terminal at the time the electric potential of the CK terminal rises.

Therefore, when the comparison signal fc changes from H→L→H→... at a predetermined period, even if the Q1 terminal of the DFF circuit 51 becomes a high level at the rise of the test signal ft, thereafter, the Q1 terminal of the DFF circuit 51 is reset at the rise of the comparison signal fc. Thus, thereafter, even if the test signal ft falls, the Q2 terminal of the DFF circuit 52 does not become a high level.

However, when there is no comparison signal fc, in other words, when the comparison signal fc does not change to a high level, the DFF circuit 51 is not reset. When the test signal ft falls, the DFF circuit 52 senses the high level signal of the Q1 terminal and outputs it as a high level signal to the Q2 terminal, and thereafter continues this operation. Note that, thereafter, when the comparison signal fc starts to change again, the Q2 terminal of the DFF circuit 52 returns to a low level.

Fig. 4 is a block diagram which illustrates the internal structure of the phase comparator 1 which is controlled by the signal detected at the comparison signal presence/absence detector 5. 11 is a phase comparing portion which is formed by an exclusive OR gate or the like, 12 is a three state buffer, 13 is an OR gate, and 14 is a switch circuit. The three state

buffer 12, the OR gate 13 and the switch circuit 14 form a control means. When the phase of the comparison signal f_c is ahead of that of the reference signal f_r , the phase comparing portion 11 makes an output terminal 11a a low level. Conversely, when the phase of the comparison signal f_c is later than that of the reference signal f_r , the phase comparing portion 11 makes the output terminal 11a a high level. The level is indefinite at times other than the times of phase comparison. Moreover, when there is a phase difference between the comparison signal f_c and the reference signal f_r , a control terminal 11b of the phase comparing portion 11 is a high level, and at other times, is a low level.

Here, the OR gate 13 takes the logical sum of a control signal outputted from the control terminal 11b of the phase comparing portion 11 and a detection signal V_a detected at the comparison signal presence/absence detector 5, and sends the logical sum to the control terminal of the buffer 12. Further, a signal of the output terminal 11a of the phase comparing portion 11 is inputted to the input side of the buffer 12 via the switch circuit 14. Moreover, the switch circuit 14 switches to the ground side (low level) when the detection signal V_a becomes a high level.

Therefore, when the detection signal V_a of the comparison signal presence/absence detector 5 is a signal-exists signal, in other words, when the detection signal V_a is low level, the buffer 12 is controlled according to the signal of the control terminal 11b of the phase comparing portion 11. Namely, during

the time in which there is a phase offset between the comparison signal f_c and the reference signal f_r , the control terminal 11b is high level. Therefore, the buffer 12 is ON such that a signal can pass between the input and the output, and the signal of the output terminal 11a of the phase comparing portion 11 is outputted as it is via the switch circuit 14, and normal operation is carried out. When there is no phase offset (at times of PLL lock), the signal of the control terminal 11b is at a low level, and the output of the buffer 12 is high impedance. Due to the signal held at the loop filter 2 which is downstream of the phase comparator 1, thereafter, the voltage control oscillator 3 oscillates a constant frequency signal.

On the other hand, when the detection signal V_a of the comparison signal presence/absence detector 5 is a signal-does-not-exist signal, in other words, when the detection signal V_a is high level, the output of the switch circuit 14 is low level, and the buffer 12 turns ON such that a signal can pass between the input and the output. Therefore, the low level signal outputted from the switch circuit 14 is outputted as it is. Accordingly, the low level signal is inputted to the loop filter 2, and the control voltage V_c which is inputted to the voltage control oscillator 4 is low level, and the frequency oscillated thereat is low.

Fig. 5 is a diagram which illustrates an operation characteristic of the voltage control oscillator 3. f_o is a target frequency of the frequency signal f_{ck} , f_{max} is an oscillation upper limit frequency, f_{min} is a oscillation lower

limit frequency, and f_{limit} is an input frequency which is an operating limit of the frequency divider 4. When the oscillation frequency f_{ck} is greater than the operating limit frequency f_{limit} , the comparison signal f_c disappears. Thus, as described above, the output signal of the phase comparator 1 is controlled to a low level, and the oscillation frequency of the voltage control oscillator 3 is controlled to a low frequency. In this way, when the oscillation frequency f_{ck} decreases and becomes less than the operating limit frequency f_{limit} , the frequency divider 4 starts to operate again, and the PLL circuit returns to original operation, and the oscillation frequency f_{ck} settles to the target frequency f_o .

In this way, in the present embodiment, even if the voltage control oscillator 3 oscillates abnormally and operation of the frequency divider 4 stops, this is sensed, and the voltage control oscillator 3 is controlled in the direction in which its oscillation frequency falls. Therefore, operation immediately returns to normal.

Fig. 6 is a block diagram which illustrates the structure of a PLL circuit of another embodiment. Here, a switch circuit 6 is connected between the frequency divider 4 and the phase comparator 1. At normal times, the switch circuit 6 is controlled such that the frequency divider 4 and the phase comparator 1 are connected to each other by the switch circuit 6. When it is detected at the comparison signal presence/absence detector 5 that there is no comparison signal, the switch circuit 6 is controlled so that a dummy pulse is inputted from

a dummy pulse generator 7 as the comparison signal f_c which is inputted to the phase comparator 1. The switch circuit 6 and the dummy pulse generator 7 form the control means.

At times of normal operation, the dummy pulse may be a signal which is a higher frequency than a frequency of the frequency signal outputted from the frequency divider 4. In this way, in the present embodiment as well, when the voltage control oscillator 3 oscillates abnormally and the operation of the frequency divider 4 stops, operation can be returned to normal immediately.

Note that in the above-described embodiments, the output signal of the phase comparator 1 is forcibly made to be a special signal (low level signal) by the detection signal V_a of the comparison signal presence/absence detector 5, or a special dummy pulse is inputted as the comparison signal to the phase comparator 1. However, the above-described embodiments are not limited to the same. For example, the control voltage V_c of the voltage control oscillator 3 may be controlled directly by the detection signal V_a of the comparison signal presence/absence detector 5 such that the oscillation frequency of the voltage control oscillator 3 is controlled to a specific low frequency. No special accuracy is demanded of this specific low frequency at this time.

Further, in the above description, the operation stoppage state of the PLL circuit is judged by the presence/absence of an output signal of the frequency divider 4. However, the operation stoppage state of the PLL circuit may be judged by

detecting by a separately provided voltage comparator whether or not the control voltage V_a of the voltage control oscillator 3 is less than or equal to a predetermined level, or by detecting whether or not the oscillation frequency f_{ck} of the voltage control oscillator 3 is a frequency of a predetermined value or more. In the latter case, the signal of the frequency f_{ck} may be converted into a voltage signal by a frequency/voltage converter, and this voltage signal compared with a predetermined value by a voltage comparator.

INDUSTRIAL APPLICABILITY

From the above, in accordance with the present invention, there is the advantage that, when an oscillation frequency of a voltage control oscillator exceeds a predetermined value and a PLL circuit stops operating, operation can return to normal quickly with a simple structure. The present invention is suitable for generation of a sampling clock of a wide range which is used when digitally processing analog image signals, and for the like.

What is claimed is:

1. A PLL circuit in which a phase comparator, a loop filter, a voltage control oscillator and a frequency divider are successively loop-connected, said PLL circuit comprising: operation stoppage detecting means for detecting that PLL operation has stopped; and control means for, when said operation stoppage detecting means detects stoppage of operation, controlling the voltage control oscillator such that an oscillation frequency of the voltage control oscillator is low.
2. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting presence/absence of an output signal of the frequency divider.
3. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting whether or not a control voltage of the voltage control oscillator is a value that oscillates a frequency which is greater than or equal to a predetermined value.
4. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting whether or not an oscillation frequency of the voltage control oscillator is value higher than a predetermined value.

5. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching an output of the phase comparator to a value at which an oscillation frequency of the voltage control oscillator decreases.

6. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching a comparison signal inputted to the phase comparator such that an oscillation frequency of the voltage control oscillator decreases.

ABSTRACT

When a voltage oscillator oscillates abnormally and a PLL circuit stops operating, in order to return to normal operation quickly, presence/absence of a comparison signal (fc) outputted from a frequency divider (4) is detected, and at times when there is no comparison signal (fc), an output signal of a phase comparator (4) is forcibly controlled to a low level temporarily, and an oscillation frequency of a voltage control oscillator (3) is decreased. The present invention is suitable for generation of a sampling clock of a wide range which is used when digitally processing analog image signals, and for the like.

FIG.1

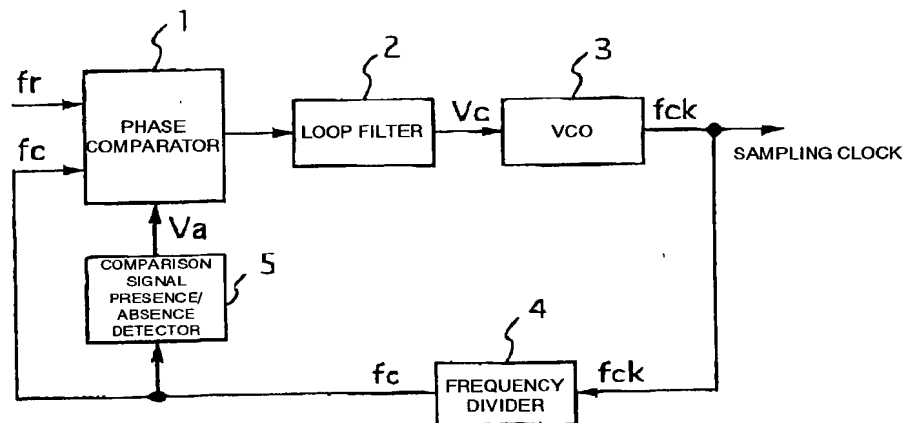


FIG.2

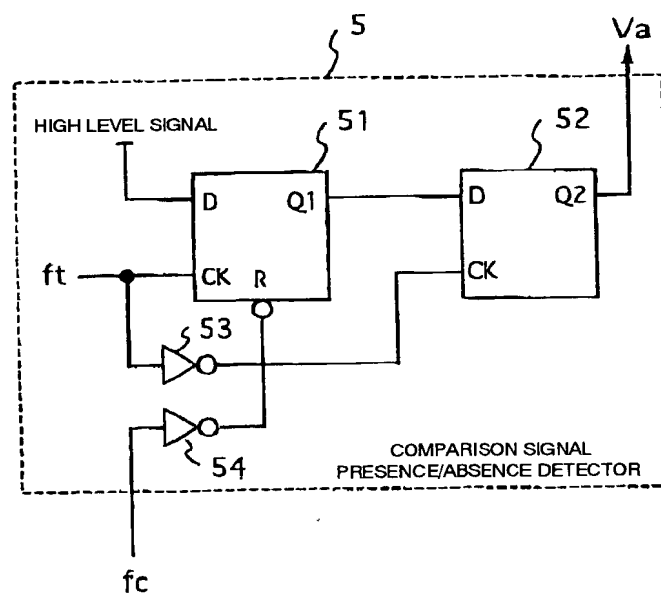


FIG.3

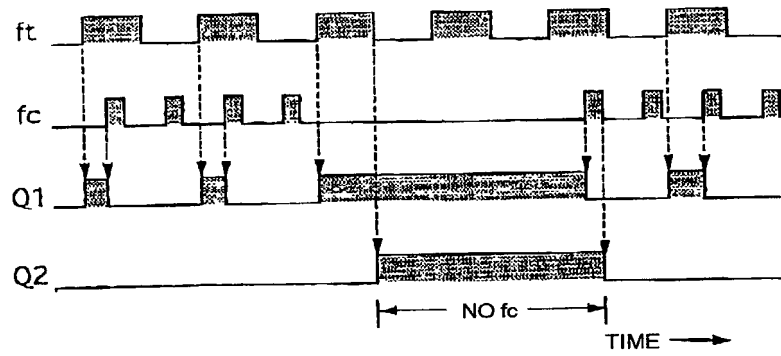


FIG.4

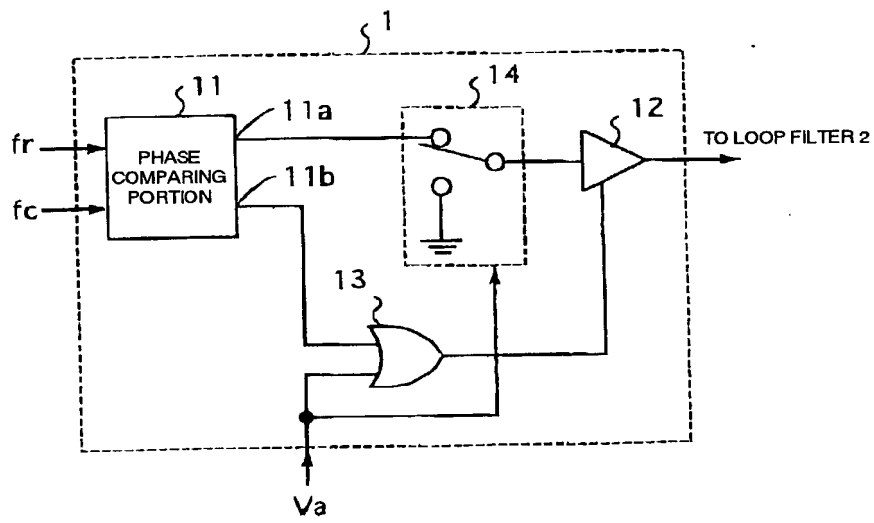


FIG.5

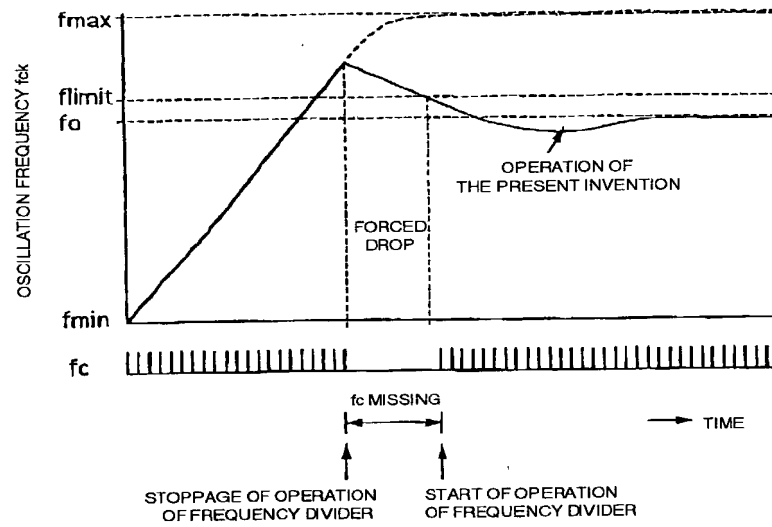


FIG.6

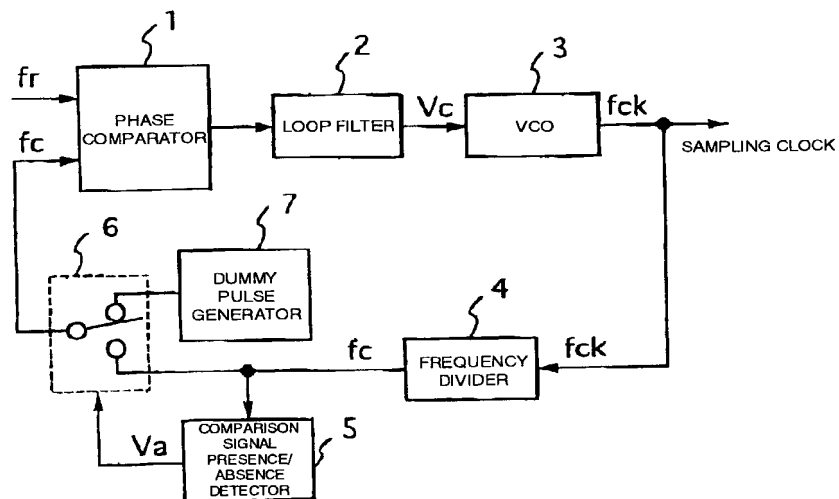


FIG.7

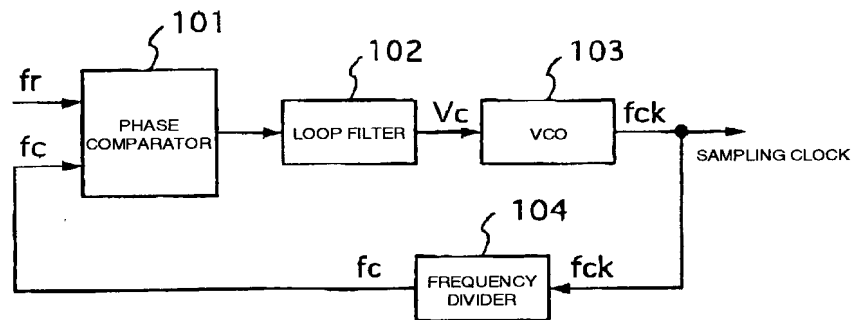


FIG.8

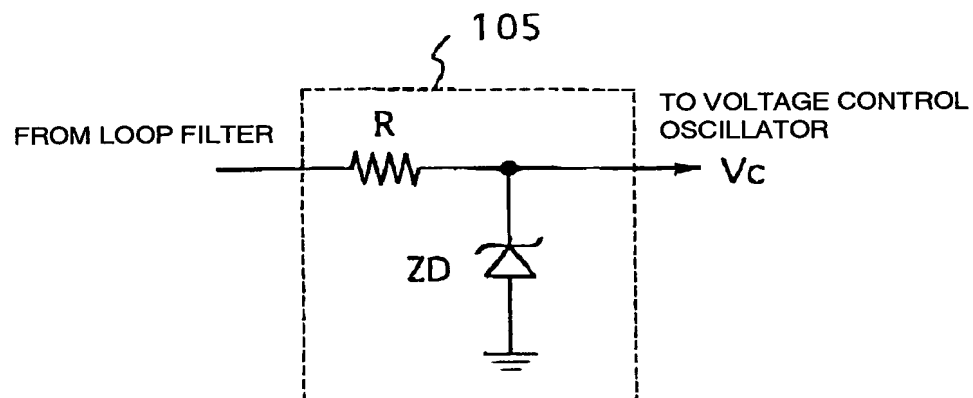
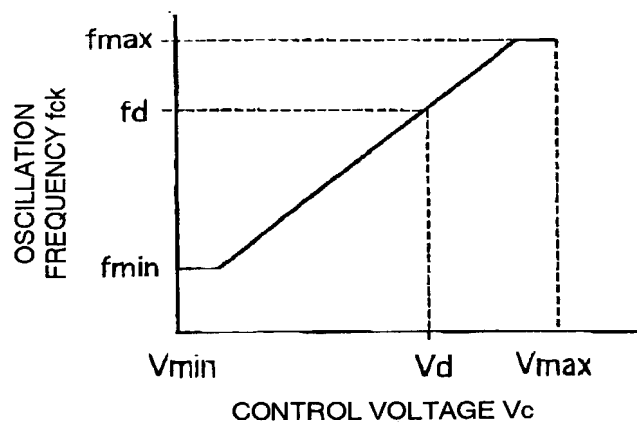


FIG.9



Declaration for U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled (Insert Title) PLL CIRCUIT
the specification of which is attached hereto unless the following is checked

☒ was filed on August 23, 2000 as PCT International Application Number PCT/JP00/05629 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed:

				Priority Claimed
(List prior foreign applications. See note A on back of this page)	<u>11/267168</u> (Number)	<u>Japan</u> (Country)	<u>21/September/1999</u> (Day/Month/Year Filed)	<u>XX</u> Yes ___ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
	_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

(See note B on back of this page)

___ See attached list for additional prior foreign applications

I hereby claim priority benefits under Title 35, United States Code, § 119 (e) of any provisional application(s) for patent listed below:

(List prior provisional applications.)	_____ (Serial Number)	_____ (Day/Month/Year Filed)
	_____ (Serial Number)	_____ (Day/Month/Year Filed)
	_____ (Serial Number)	_____ (Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(List Prior U.S.
Applications)

(Appln. Serial No.)

(Filing Date)

(Status: Patented, Pending, Abandoned)

(Appln. Serial No.)

(Filing Date)

(Status: Patented, Pending, Abandoned)

(Appln. Serial No.)

(Filing Date)

(Status: Patented, Pending, Abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:



23850

PATENT TRADEMARK OFFICE

Please direct all communications to the following address:



23850

PATENT TRADEMARK OFFICE

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See note C
above)

Full name of sole or first inventor (given name, family name) Takushi KIMURA

Inventor's signature Takushi Kimura Date July 3, 2001

Residence Kawasaki, Japan JPX Citizenship Japanese

Post Office Address c/o FUJITSU GENERAL LTD. 1116, Suenaga, Takatsu-Ku, Kawasaki-Shi,
Kanagawa 213-8502, Japan

Full name of second inventor (given name, family name) Masamichi NAKAJIMA

Inventor's signature Masamichi Nakajima Date July 3, 2001

Residence Kawasaki, Japan JPX Citizenship Japanese

Post Office Address c/o FUJITSU GENERAL LTD. 1116, Suenaga, Takatsu-Ku, Kawasaki-Shi,
Kanagawa 213-8502, Japan

Full name of third inventor (given name, family name) _____

Inventor's signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fourth inventor (given name, family name) _____

Inventor's signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fifth inventor (given name, family name) _____

Inventor's signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____